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Pre-Lab #10

11-14-22

1. Binary numbers for 13, 7, and 9.

13 – 1101

7 - 0111

9 – 1001

1. The completed state diagram for the combinational-lock FSM.

Diagram

Description automatically generated

1. The combinational-lock FSM Verilog module. Refer to the above sections to complete this.

`timescale 1ns / 2ns

`default\_nettype none

module combination\_lock\_fsm(

output reg [2:0] State,

output reg [2:0] nextState,

output wire Locked,

input wire Right, Left,

input wire [4:0] Count,

input wire Center,

input wire Clk, South,

parameter S0: 3'b000,

S1: 3'b001,

S2: 3'b010,

S3: 3'b011,

S4: 3'b010

);

always@(\*)

case ( State )

S0: begin

if (right == 1)

nextstate = S1;

else

nextState = S0;

end

S1: begin

if (right == 1 && Count == 7)

nextState = S3;

else if (Center == 1 && Count != 17)

nextState = S0;

end

S4: begin

Locked = 0;

end

endcase

always@(posedge Clk)

if( South )

State <= S0;

else

State <= nextState;

endmodule